LM26001 Evaluation Board

National Semiconductor
Application Note 1454
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Introduction

The LM26001 evaluation board is designed to demonstrate the capabilities of the LM26001 switching regulator.

The LM26001 board, schematic shown in Figure 1, is configured to provide an output of 3.3V at up to 1.5A from an input range of 3.5V to 38V (a minimum of 4.5V is required for startup). The nominal operating frequency is 305 kHz and can be synchronized from +30% to -20% of nominal using the SYNC connection post. The evaluation board is designed to operate at ambient temperatures up to 75˚C.

Typical evaluation board waveforms and performance curves are shown in Figures 2 through 7. Figures 8 and 9 show the pcb trace layout. To aid in the design and evaluation of dc/dc buck converters based on the LM26001 regulator, the evaluation board can be re-configured for different output voltages and operating frequencies. Test points are also provided to enable easy connection and monitoring of critical signals.

Table 2 shows the BOM for a second example circuit for 1.5V output and 480 kHz switching frequency. This design operates from an input voltage of 3.5V to 38V and enters pulse skipping mode at approximately 24Vin, depending on loading.

For more information about device function and circuit design, refer to the LM26001 datasheet.

Jumper Settings

The **FPWM** jumper is used to disable the sleep mode function. For normal operation, select 'off', which connects FPWM to GND. For FPWM operation (sleep mode disabled), select 'on'. The **Vbias** jumper connects the VBIAS pin to Vout. When Vout is greater than 3V, the VBIAS function will be activated for improved efficiency. To disable VBIAS, or if Vout is set to less than 3V, set the jumper to 'GND'.

Optional Components

Before changing the default components, please refer to the product datasheet for information regarding component selection.

Output voltage and frequency are easily adjustable with single resistors, **R1** and **R3** respectively. However, large changes to the default settings may require other changes to the inductor, output capacitor, and compensation network.

Several optional component pads have been provided for application flexibility.

The **C7** pad is provided for an additional ceramic output capacitor. This capacitor can be used to lower the total ESR at the output. **D2** blocks reverse current to the input supply during low input voltage and light load conditions. This diode may not be necessary in all applications and can be replaced with a jumper.

C10 is a phase lead capacitor which can be installed to increase phase and gain margin. See the compensation section of the datasheet for more detailed information.

Powering Up

Before powering up the LM26001 evaluation board, all external connections should be verified. The power supply input must be turned off and connected with proper polarity to the VIN and GND posts. The load should be connected between the VOUT post and GND post. Both the VIN and VOUT connections should use the GND post closest to the VIN post. Output voltage can be monitored with a DVM or oscilloscope at the VOUT post.

The second GND post, close to the IC, is provided primarily for small signal measurements, such as soft-start voltage, or PGOOD. This GND post should also be used when applying optional external signals such as EN and SYNC.

Once all connections have been verified, input power can be applied. The input voltage must be set between 4.5V and 38V. The load can be on or off at startup. If the EN post is left open, the output voltage will ramp up when VIN is applied

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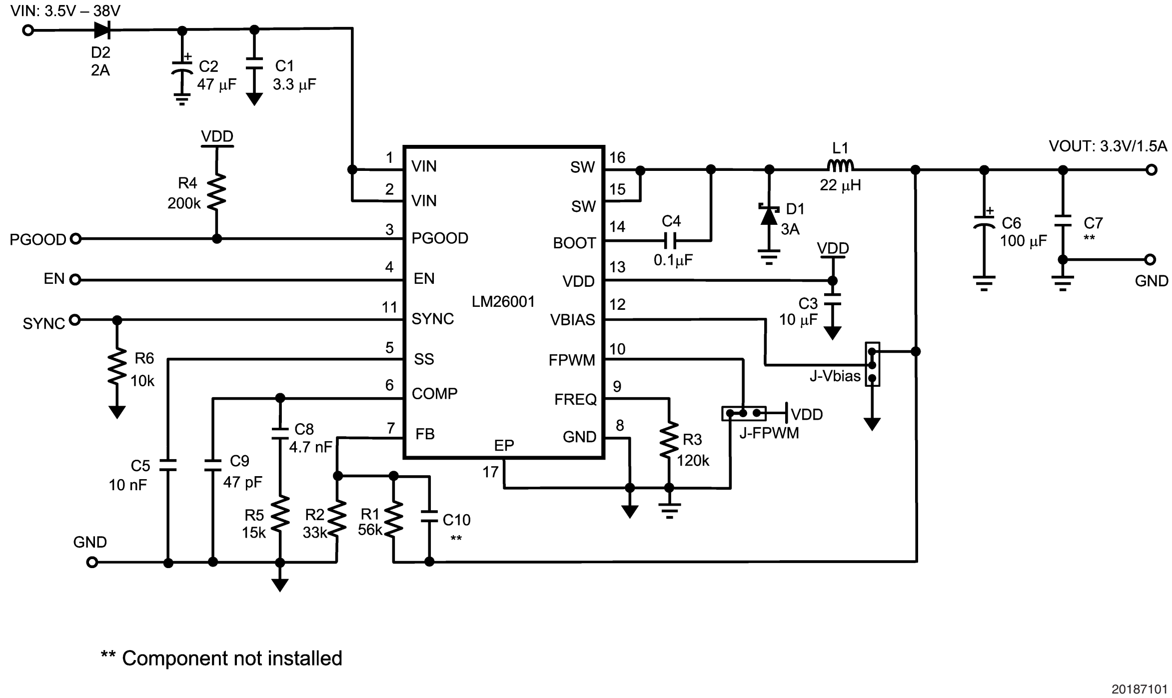

FIGURE 1. Evaluation Board Schematic

TABLE 1. LM26001 Bill of Materials for V_O = 3.3V, 1.5A, 305kHz

Ref #	Value	Footprint	Supplier
C1	3.3µF 50V X7R ceramic	1210	TDK
C2	47µF 50V low ESR electrolytic		Panasonic
C3	10µF 10V B ceramic	1206	Murata
C4	0.1µF 50V COG ceramic	1206	Murata
C5	10nF 50V X7R ceramic	0603	Murata
C6	100µF 8V 12mohm SP		Panasonic
C7	not installed	1206	-
C8	4.7nF 50V COG ceramic	0603	Murata
C9	47pF 50V COG ceramic	0603	Murata
C10	not installed	0603	-
D1	60V 3A NSQ03A06	SMC	NIEC
D2	60V 2A EC21QS06	SMA	NIEC
L1	22µH 3.5A SLF12565T-220M3R5		TDK
R1	56kΩ 1%	0603	-
R2	33kΩ 1%	0603	-
R3	120kΩ 1%	0603	-
R4	200kΩ 5%	0603	-
R5	15kΩ 1%	0603	-
R6	10kΩ 5%	0603	-

Performance Characteristics

Unless otherwise specified, VIN = 12V, T_A = 25˚C.

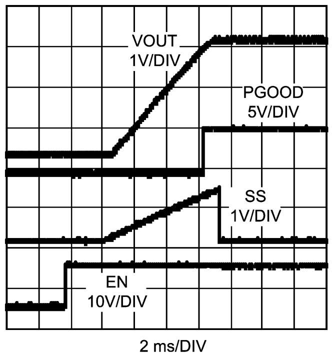

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FIGURE 2. Start-Up Waveforms (I_{OUT} = 1A)

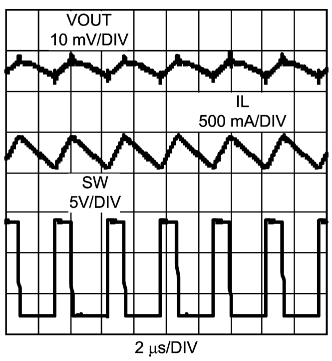

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FIGURE 3. PWM Waveforms (I_{OUT} = 1A)

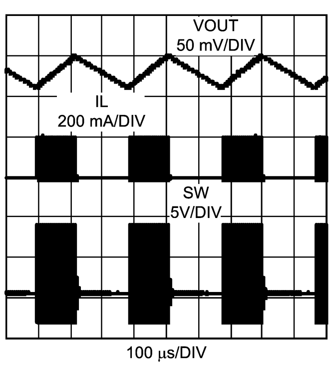

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FIGURE 4. Sleep Mode Waveforms (I_{OUT} = 25mA)

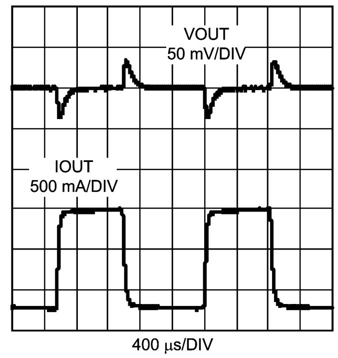

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FIGURE 5. Load Transient Response (I_{OUT} = 0.25A to 1.5A step)

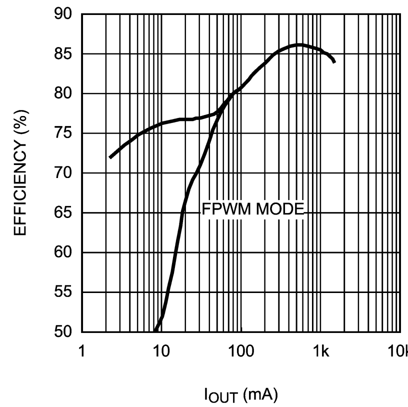

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FIGURE 6. Efficiency vs I_{OUT} (V_{BIAS} = V_{OUT})

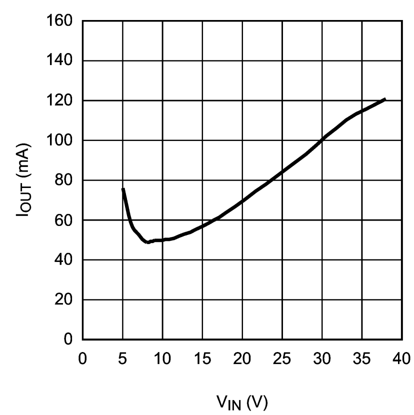

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FIGURE 7. Sleep Mode Threshold Load Current vs Input Voltage

PCB Layout Diagram(s)

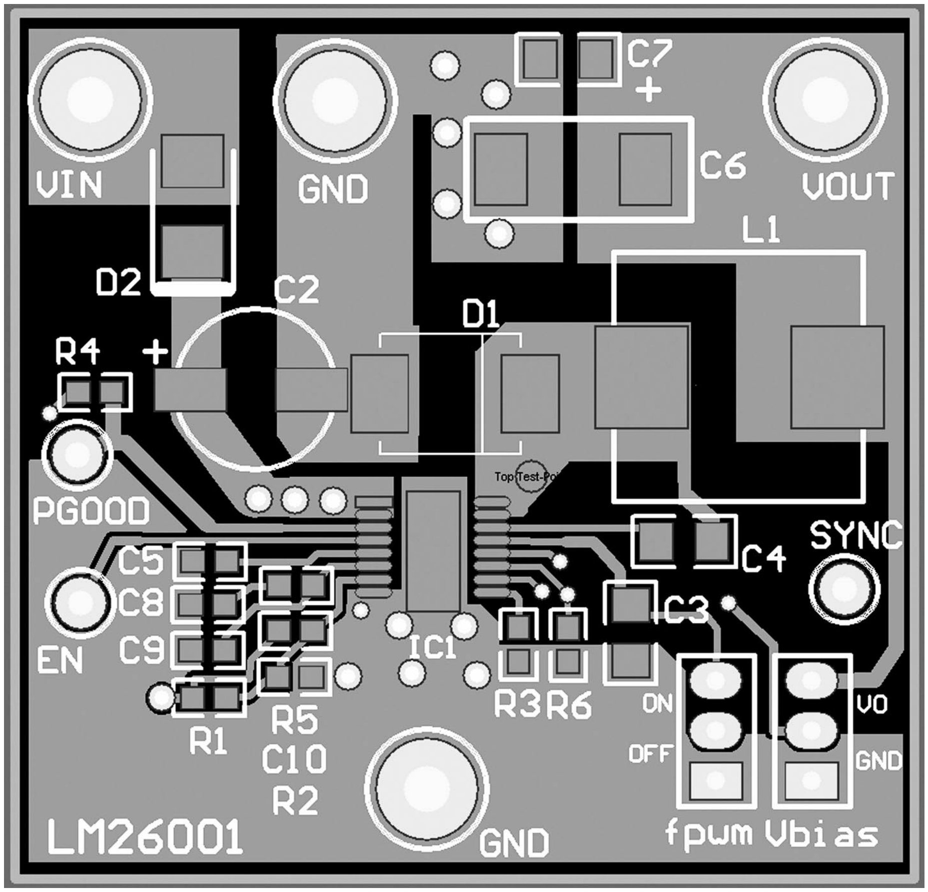

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FIGURE 8. Top Side Layout

PCB Layout Diagram(s) (Continued)

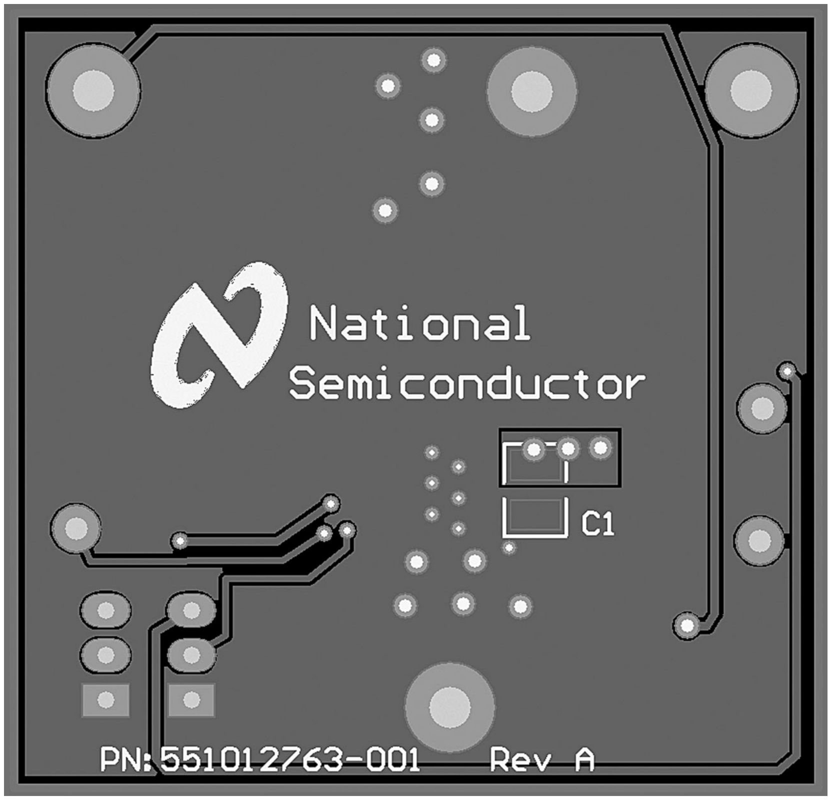

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FIGURE 9. Bottom Side Layout

TABLE 2. LM26001 Bill of Materials for V_O = 1.5V, 1.5A, 480kHz

Ref #	Value	Footprint	Supplier
C1	3.3µF 50V X7R ceramic	1210	TDK
C2	47µF 50V electrolytic		Panasonic
C3	10µF 10V B ceramic	1206	Murata
C4	0.1µF 50V COG ceramic	1206	Murata
C5	10nF 50V X7R ceramic	0603	Murata
C6	100µF 8V 12mohm SP		Panasonic
C7	10µF 6.3V X7R ceramic	1206	Murata
C8	6.8nF 16V COG ceramic	0603	Murata
C9	68pF 25V COG ceramic	0603	Murata
C10	not installed	0603	-
D1	60V 3A NSQ03A06	SMC	NIEC
D2	60V 2A EC21QS06	SMA	NIEC
L1	3.3µH 4.1A RLF7030T-3R3M4R1		TDK
R1	8.2kΩ 1%	0603	-
R2	39kΩ 1%	0603	-
R3	75kΩ 1%	0603	-
R4	200kΩ 5%	0603	-
R5	20kΩ 1%	0603	-
R6	10kΩ 5%	0603	-

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